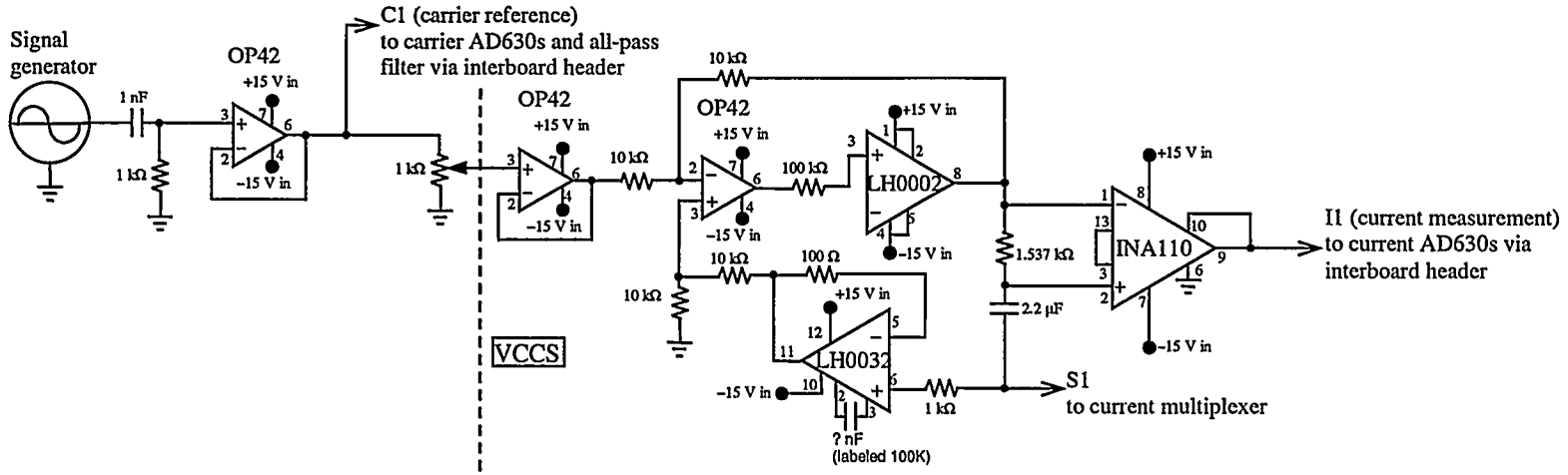
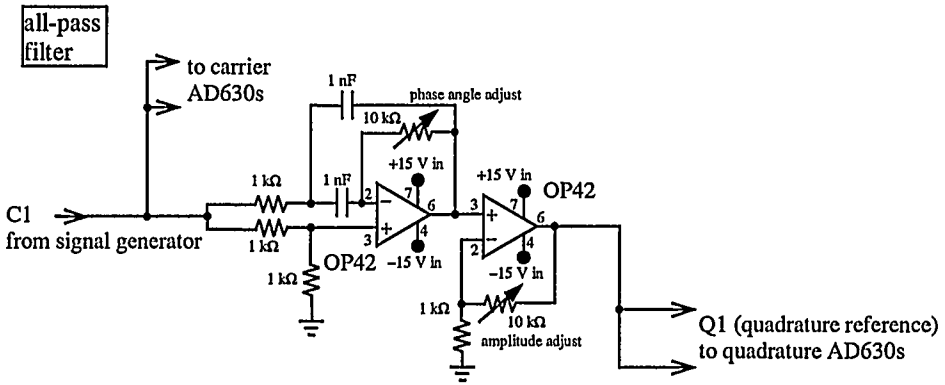
Appendix A
Circuit Diagrams of the Sandia/Michigan EIT System

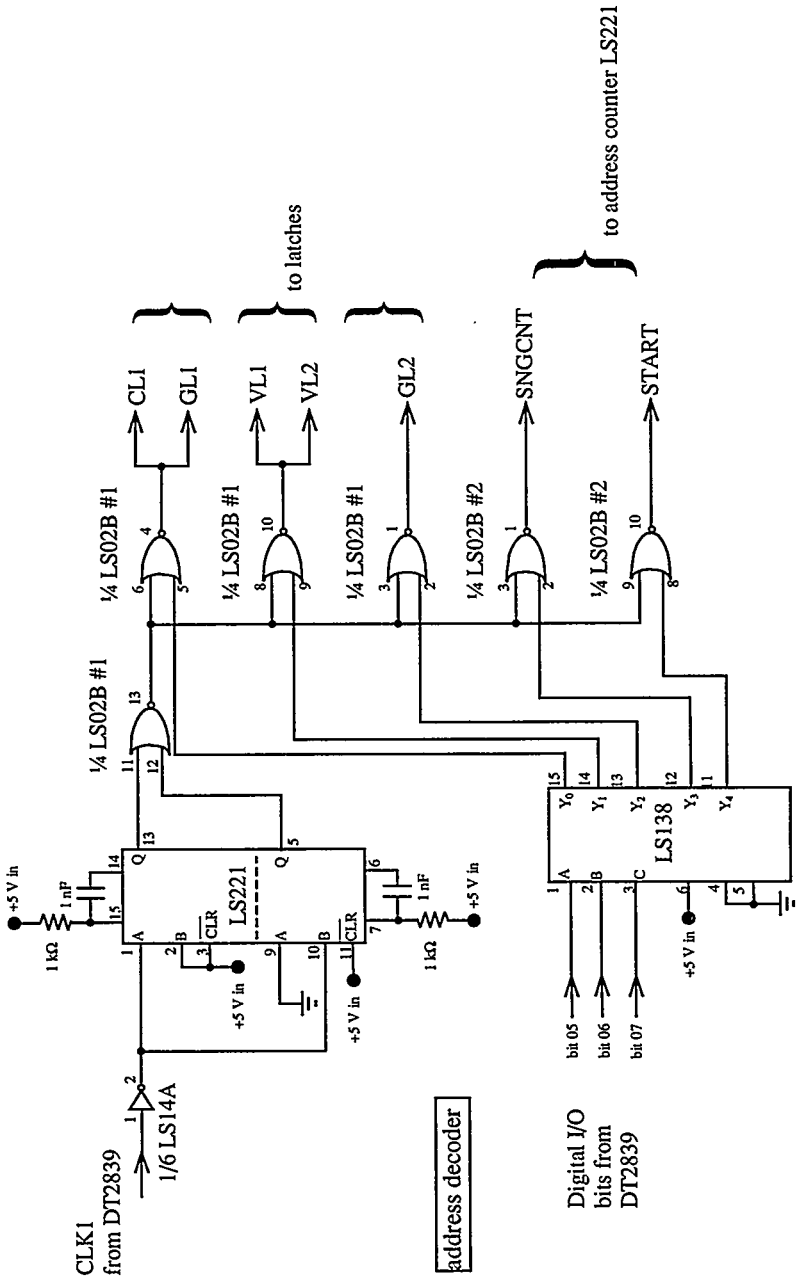
The following pages present circuit diagrams for the custom-built portion of the Sandia/Michigan EIT system. The first portion contains diagrams for circuitry in the EIT package, including:

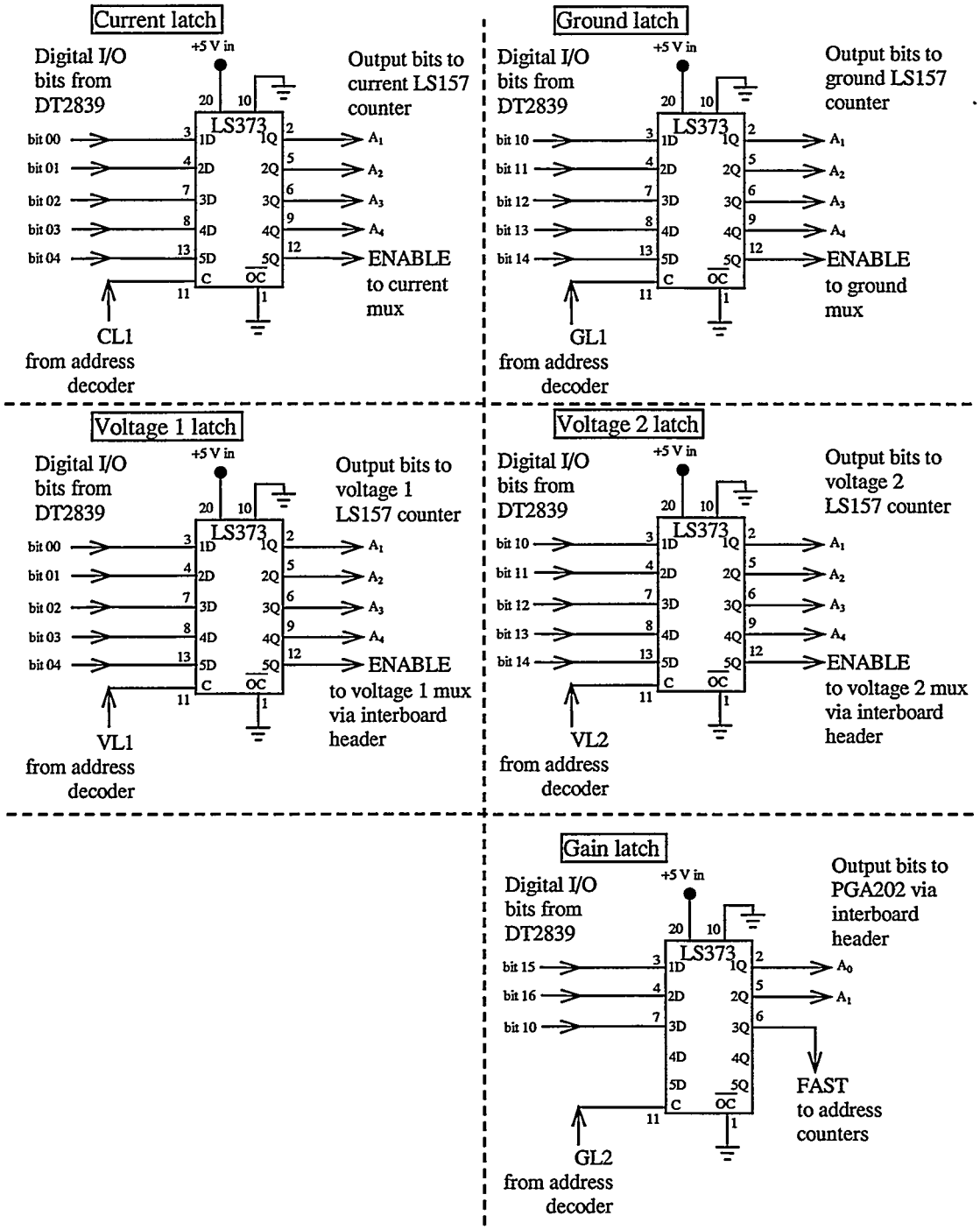
- circuitry to generate reference signals and injection current
- address decoders to initialize latches and electrode counters
- latches to select injection, ground and measurement electrodes from "slow mode" computer commands
- internal counters to select electrodes in "fast mode"
- multiplexers and buffers to and from electrodes
- amplifier, demodulators and low pass filters to process measured voltage signals

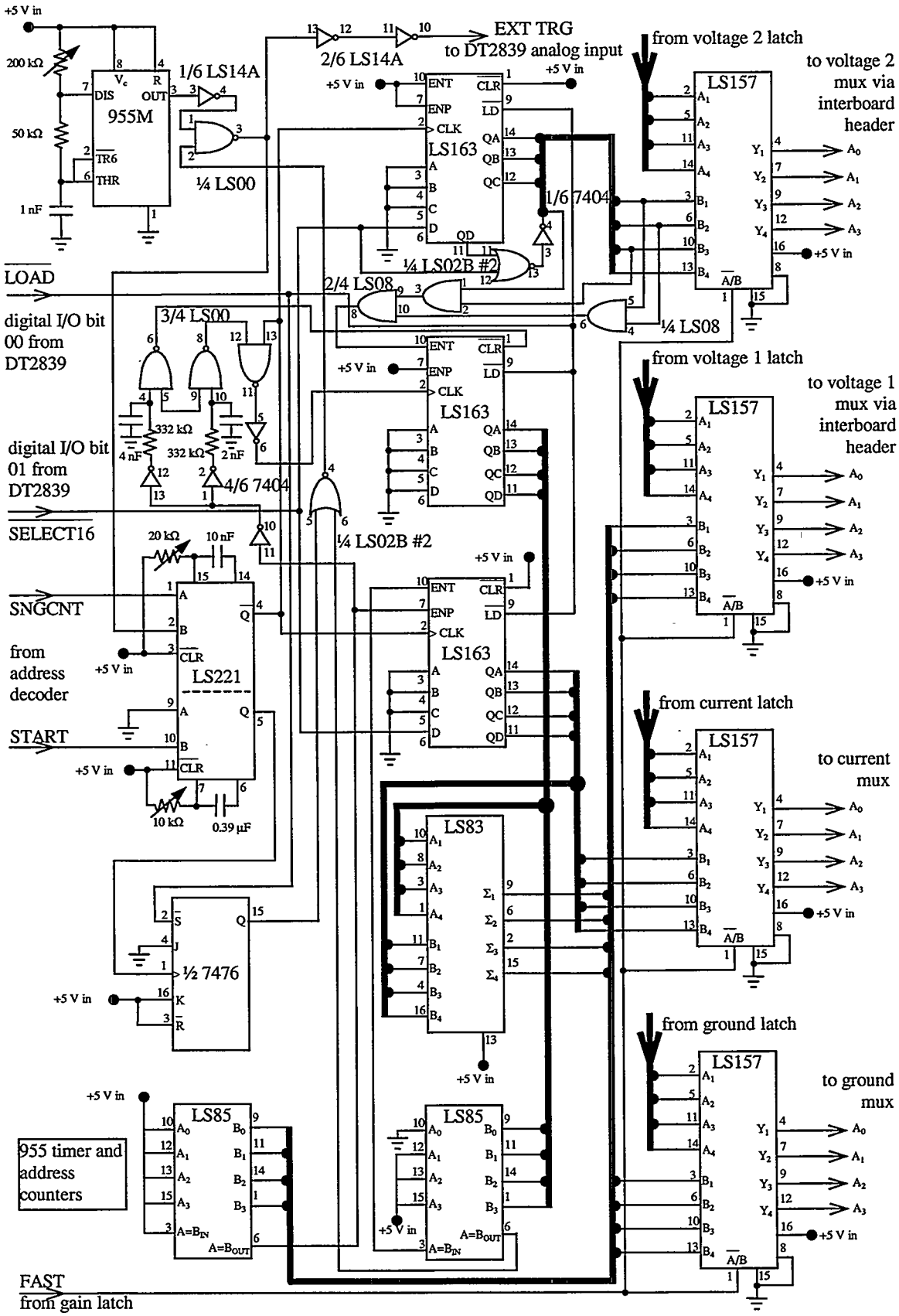
Labeled arrows mark connections between circuits on different pages. The circuit schematics are followed by diagrams of header connections between circuit boards, electrodes and the DT2839 data acquisition board.

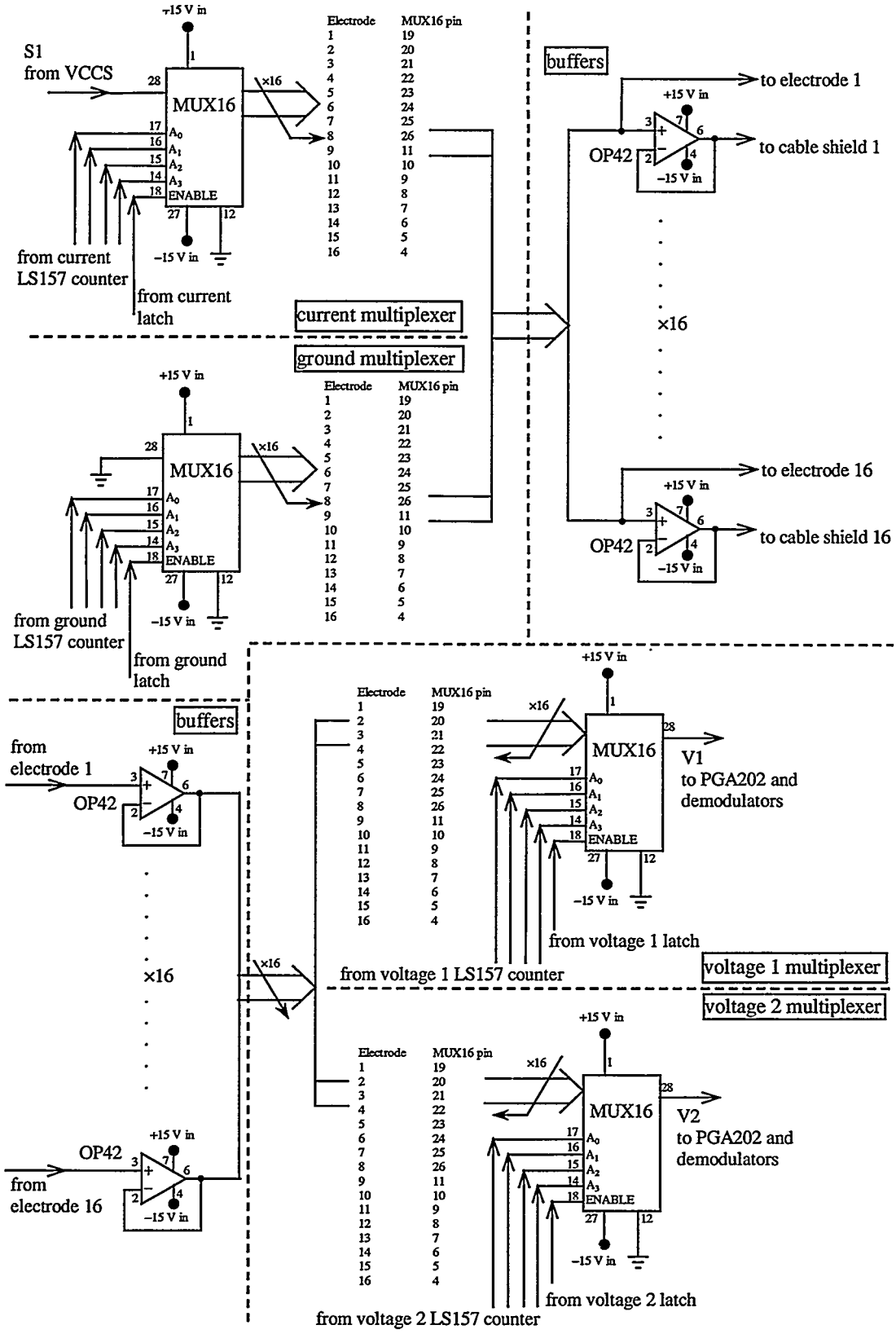

Signal generator
1 nF
1 kΩ
OP42
+15 V in
-15 V in
C1 (carrier reference)
to carrier AD630s and all-pass
filter via interboard header
1 kΩ
OP42
+15 V in
-15 V in
10 kΩ
VCCS
OP42
+15 V in
-15 V in
10 kΩ
100 kΩ
LH0002
+15 V in
-15 V in
10 kΩ
100 Ω
10 kΩ
LH0032
+15 V in
-15 V in
1 kΩ
? nF
(labeled 100K)
1.537 kΩ
2.2 µF
INA110
+15 V in
-15 V in
I1 (current measurement)
to current AD630s via
interboard header
S1
to current multiplexer

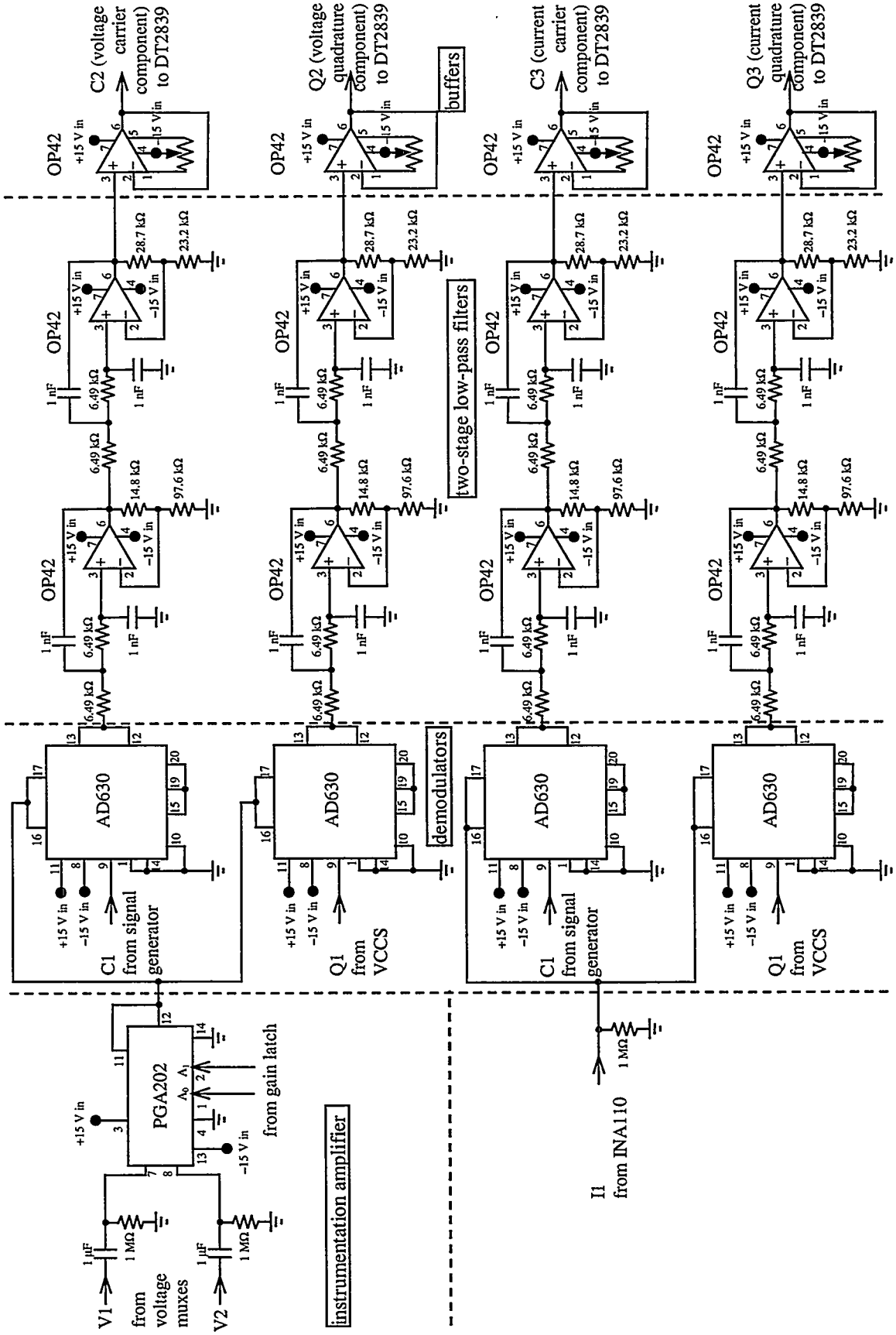

all-pass filter
to carrier AD630s
C1
from signal generator
1 nF
phase angle adjust
10 kΩ
+15 V in
1 kΩ
1 nF
1 kΩ
OP42
-15 V in
1 kΩ
+15 V in
OP42
-15 V in
1 kΩ
10 kΩ
amplitude adjust
Q1 (quadrature reference)
to quadrature AD630s


CLK1
from DT2839
1/6 LS14A
address decoder
Digital I/O
bits from
DT2839
bit 05
bit 06
bit 07
LS138
LS221
+5 V in
1 kΩ
1 nF
¼ LS02B #1
¼ LS02B #2
to latches
to address counter LS221
CL1
GL1
VL1
VL2
GL2
SNGCNT
START


Current latch
Digital I/O bits from DT2839
+5 V in
LS373
bit 00
bit 01
bit 02
bit 03
bit 04
Output bits to current LS157 counter
ENABLE to current mux
CL1 from address decoder
Ground latch
Digital I/O bits from DT2839
bit 10
bit 11
bit 12
bit 13
bit 14
Output bits to ground LS157 counter
ENABLE to ground mux
GL1 from address decoder
Voltage 1 latch
Digital I/O bits from DT2839
Output bits to voltage 1 LS157 counter
ENABLE to voltage 1 mux via interboard header
VL1 from address decoder
Voltage 2 latch
Digital I/O bits from DT2839
Output bits to voltage 2 LS157 counter
ENABLE to voltage 2 mux via interboard header
VL2 from address decoder
Gain latch
Digital I/O bits from DT2839
bit 15
bit 16
Output bits to PGA202 via interboard header
FAST to address counters
GL2 from address decoder


+5 V in
200 kΩ
50 kΩ
1 nF
955M
1/6 LS14A
¼ LS00
2/6 LS14A
EXT TRG
to DT2839 analog input
LS163
1/6 7404
¼ LS02B #2
2/4 LS08
¼ LS08
LOAD
digital I/O bit 00 from DT2839
3/4 LS00
digital I/O bit 01 from DT2839
332 kΩ
4 nF
2 nF
4/6 7404
SELECT16
20 kΩ
10 nF
SNGCNT
from address decoder
START
LS221
10 kΩ
0.39 µF
½ 7476
LS83
LS85
955 timer and address counters
FAST
from gain latch
from voltage 2 latch
to voltage 2 mux via interboard header
LS157
from voltage 1 latch
to voltage 1 mux via interboard header
from current latch
to current mux
from ground latch
to ground mux

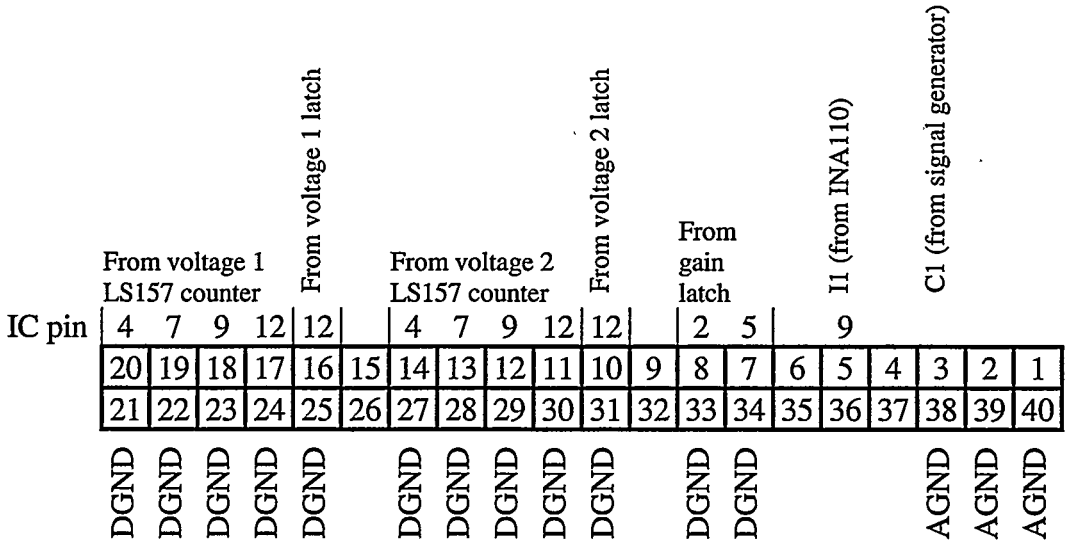

+15 V in
S1
from VCCS
MUX16
×16
ENABLE
−15 V in
from current
LS157 counter
from current
latch
current multiplexer
ground multiplexer
from ground
LS157 counter
from ground
latch
Electrode
MUX16 pin
buffers
to electrode 1
to cable shield 1
to electrode 16
to cable shield 16
OP42
from
electrode 1
from
electrode 16
V1
to PGA202 and
demodulators
V2
to PGA202 and
demodulators
from voltage 1 latch
from voltage 1 LS157 counter
from voltage 2 latch
from voltage 2 LS157 counter
voltage 1 multiplexer
voltage 2 multiplexer


V1
from voltage muxes
V2
1 µF
1 MΩ
PGA202
+15 V in
−15 V in
from gain latch
instrumentation amplifier
I1
from INA110
1 MΩ
AD630
C1 from signal generator
Q1 from VCCS
demodulators
OP42
1 nF
6.49 kΩ
14.8 kΩ
97.6 kΩ
two-stage low-pass filters
28.7 kΩ
23.2 kΩ
buffers
C2 (voltage carrier component) to DT2839
Q2 (voltage quadrature component) to DT2839
C3 (current carrier component) to DT2839
Q3 (current quadrature component) to DT2839

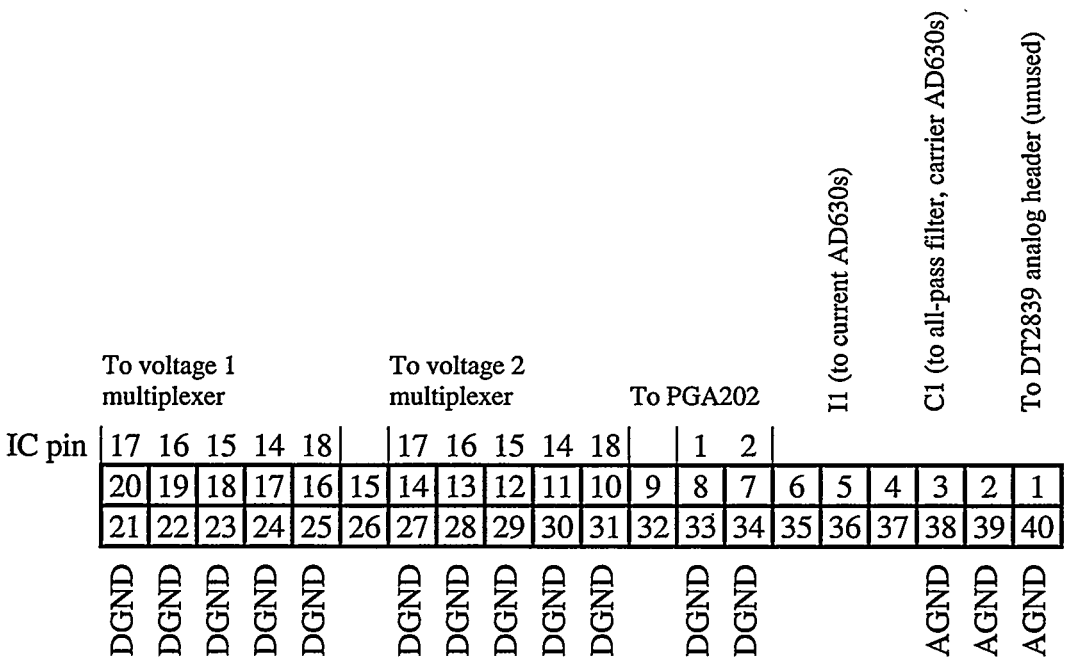
Interboard header

Numbered boxes represent header pins; DGND = digital ground; AGND = analog ground

Board 1 header



Board 2 header



Headers between multiplexers and electrodes

Header from board 1 to electrode cable screw terminals

Lines 17 – 48 unused

From current and ground multiplexers

mux pin					4	5	6	7	8	9	10	11	26	25	24	23	22	21	20	19
	·	·	·	·	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	·	·	·	·	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
electrode					16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

From shield drivers

Header from electrode cable screw terminals to board 2

Lines 1 – 48 unused

·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	
electrode				16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

To voltage buffers

Headers between DT2839 and EIT electronics

Header between DT2839 digital I/O terminals and board 1

	EXT TRG pulse to DT2839	CLK1 pulse to address decoder				To LS138 (address decoder)			To latches											
Digital I/O bit						07	06	05	16	15	14	13	12	11	10	04	03	02	01	00
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
	DGND				DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND

Header between DT2839 analog I/O terminals and board 2

To pin 40, board 2, interboard header	1	16	To pin 1, board 2, interboard header	
	2	15		
	3	14	Q3, current quadrature	Voltage components measured by DT2839
	4	13	C3, current carrier	
AGND	5	12	Q2, voltage quadrature	
	6	11		
	7	10		
AGND	8	9	C2, voltage carrier	